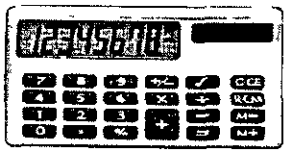
UNIVERSITY EXAMINATIONS



UNIVERSITEITSEKSAMENS

UNISA university of south africa

DIG1501

May/June 2015

DIGITAL SYSTEMS I (THEORY)

Duration 3 Hours

100 Marks

EXAMINERS .
FIRST MR PO UMENNE
SECOND MR NR NETSHIKWETA

Programmable pocket calculator is permissible

Closed book examination

This examination question paper remains the property of the University of South Africa and may not be removed from the examination venue

This examination question paper consists of 8 pages including the cover page

Answer all the questions

PLEASE NOTE: IF YOU HAVE THE OPINION THAT INSUFFICIENT INFORMATION IS SUPPLIED FOR YOU TO ANSWER A PARTICULAR QUESTION, MAKE A REALISTIC ASSUMPTION, MOTIVATE IT AND THEN ANSWER THE QUESTION.

NUMBER SYSTEMS OPERATION AND CODES

QUESTION 1

1 1 Determine the 1's complement of the binary number

11010111 (2)

1 2 Determine the 2's complement of the binary number

10110000 (2)

1.3 Express the decimal number as an 8-bit number in the 1's complement form

-34 (2)

1.4 Express the decimal number as an 8-bit number in the 2's complement form.

-68 (2)

1 5 Determine the decimal value of the signed binary number in the 1's complement from 10111111 (2)

1 6 Determine the decimal value of the signed binary number in the 2's complement form 10011001 (2)

[12]

LOGIC GATES

QUESTION 2

2 1 Derive a truth table for the gate below to help you with the waveform. (4)

2 2 Determine the gate output for the input waveforms in figure 1 and draw the timing diagram (4)

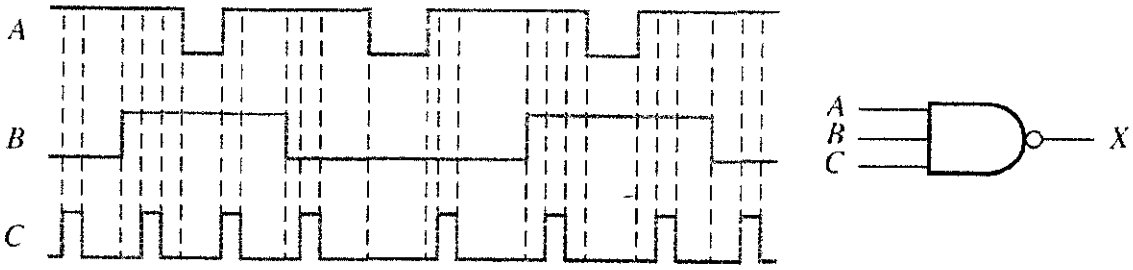


Figure 1

[8]

QUESTION 3

Sensors are used to monitor the pressure and the temperature of a chemical solution stored in a vat The circuitry for each sensor produces a HIGH voltage when a specified maximum value is exceeded An alarm requiring a LOW voltage input must be activated when either the pressure or the temperature is excessive Design a circuit for this application

3.1 Sketch a truth Table first (4)

3 2 Sketch the circuit with logic gates showing the alarm (4)

[8]

BOOLEAN ALGEBRA AND LOGIC SIMPLIFICATION

QUESTION 4

4 1 Apply DeMorgan's Theorems to the following expression

$$\overline{\overline{A + B\bar{C} + D(\overline{E + \bar{F}})}} \quad (4)$$

4 2 The Boolean expression for an exclusive-OR gate is $A\bar{B} + \bar{A}B$ With this as a starting point, use DeMorgan's theorems and any other rules or laws that are applicable to develop an expression for the exclusive-NOR gate from the expression below

$$\overline{A\bar{B} + \bar{A}B} \quad (5)$$

4 3 Simplify the following Boolean expression using Boolean algebra

$$\overline{AB + A\bar{C}} + \bar{A}\bar{B}C \quad (7)$$

4.4 Convert the following Boolean expression into standard POS form

$$(A + \bar{B} + C)(\bar{B} + C + \overline{D})(A + \bar{B} + \bar{C} + D) \quad (4)$$

4.5 Convert the following SOP expression to an equivalent POS expression

$$\bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC \quad (4)$$

[24]

KARNAUGH MAP SIMPLIFICATION

QUESTION 5

5 1 Use a Karnaugh map to simplify the following SOP expression (remember to make it standard first)

$$\bar{W}\bar{X}\bar{Y}\bar{Z} + W\bar{X}YZ + W\bar{X}\bar{Y}Z + \bar{W}YZ + W\bar{X}\bar{Y}\bar{Z} \quad (8)$$

5 2 In a 7-segment display, each of the seven segments is activated for various digits For example, segment a is activated for the digits 0,2,3,5,6,7,8, and 9, as illustrated in figure 2 Since each digit can be represented by a BCD code

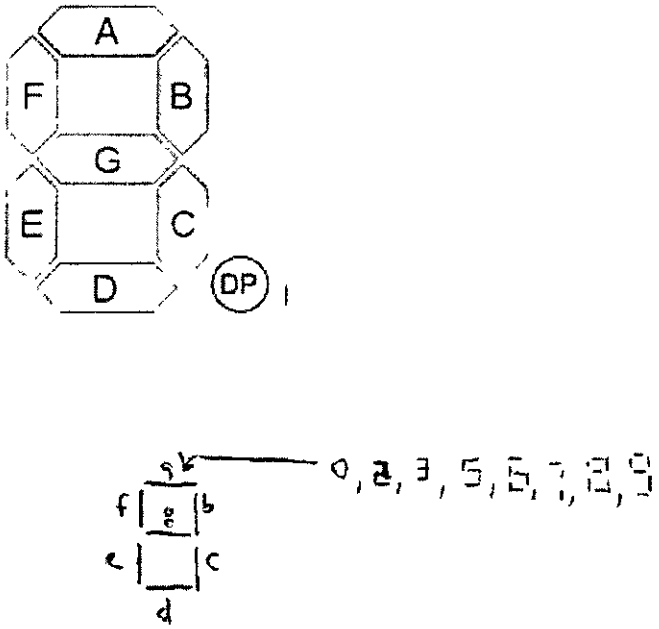


Figure 2

5 2 1 Derive a truth table for segment a using the variables ABCD (4)

5 2 2 Derive an SOP expression for segment a and then (4)

5 2 3 Minimize the expression using a Karnaugh map (8)

5 2 4 Draw the logic diagram for the segment-a logic (5)

[29]

Consider don't cares ('X')

COMBINATIONAL LOGIC ANALYSIS

QUESTION 6

6 1 For the following Boolean expression implement the expression using only NAND gates (HINT double complement and use De-Morgans theorem to expand) (8)

$$(AB + \bar{C})D + EF$$

6.2 Implement the expression with ONLY NAND gates and sketch the circuit diagram. (5)

[13]

FUNCTIONS OF COMBINATIONAL LOGIC

QUESTION 7

The waveforms in figure 3 below are observed on the inputs of a 74LS151 8-input multiplexer shown in figure 4 Remember that when the enable is not active the output is LOW

7 1 Sketch the truth table for the Y output (4)

7.2 Sketch the Y output waveform. (2)

[6]

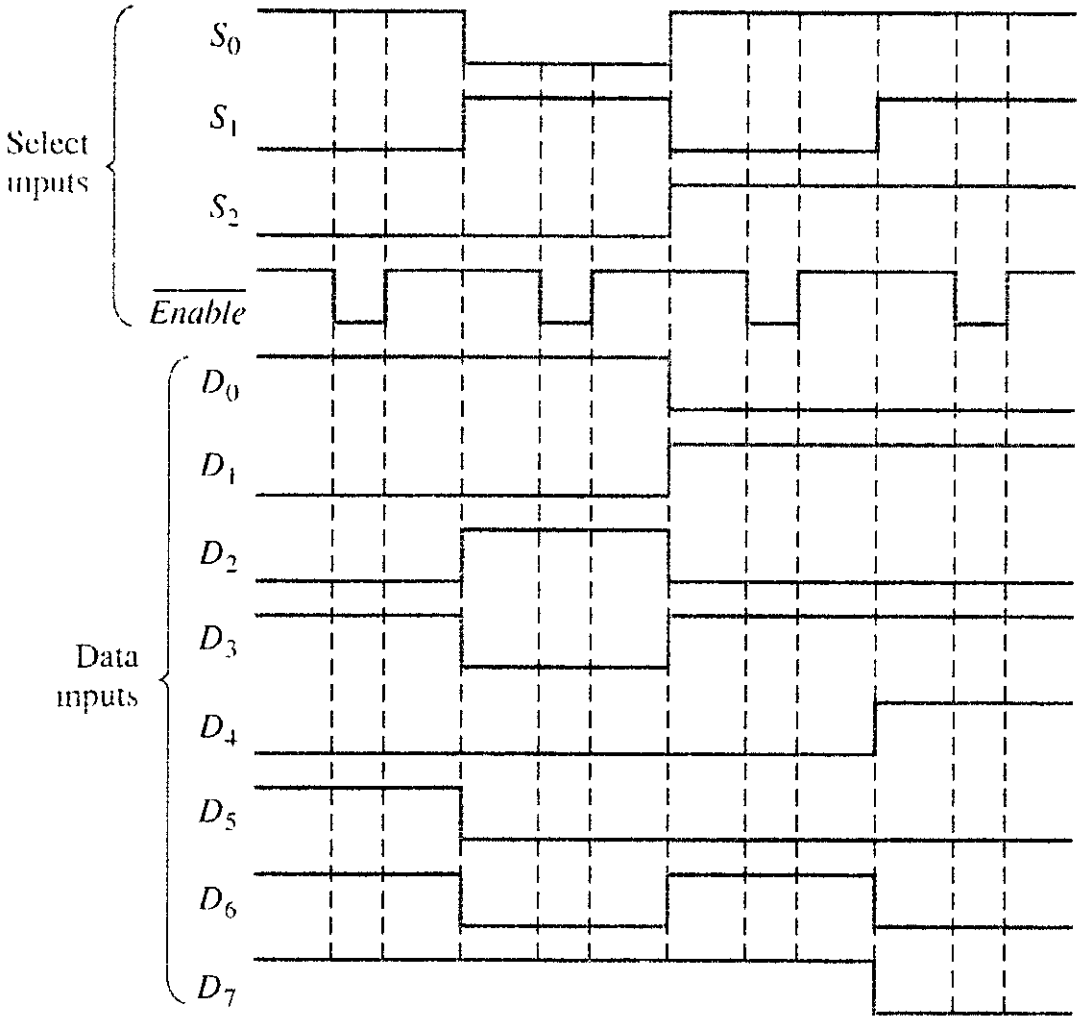


Figure 3

[TURN OVER]

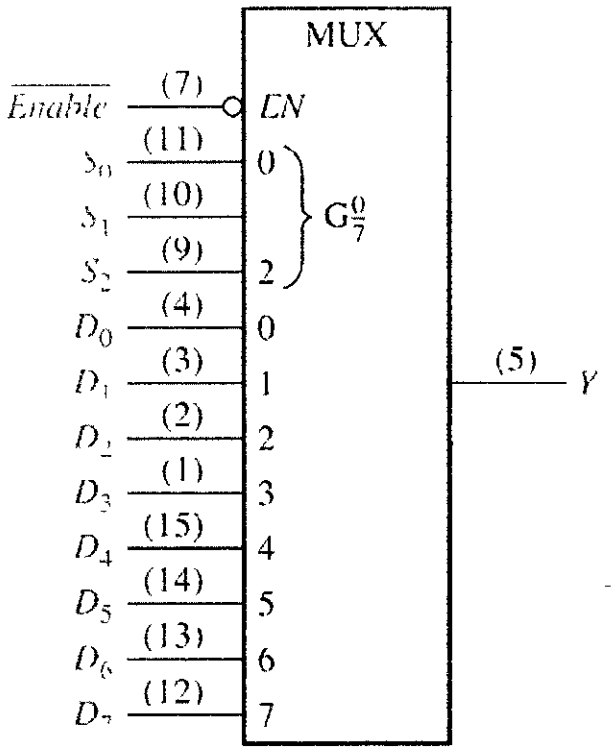


Figure 4

TOTAL: 100