# October / November 2012

**Question 2(a)** (5)

To improve performance, designers have turned to a fundamentally new approach to chip organization and architecture, called *multicore* organization. Explain what this means and list four of the advantages of using this approach.

Multicore - Multiple processors on the same chip - with a large shared cache.

- increases performance without increasing the clock rate;
- justifies much larger caches;
- results in lower power consumption and less heat generation;
- uses multiple simpler processors, rather than more complex one.

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**Question 2(b)** (5)

List and describe the most common classes of interrupt.

- **Program interrupts** - occur as the result of the execution of an instruction, such as division by 0, arithmetic overflow etc.

- **Timer interrupts** - generated by a timer within the processor. Allows the operating system to perform certain functions on a regular basis.

- **I/O interrupts** - generated by an I/O controller, to signal the normal completion of an operation, or an error condition.

- **Hardware failure** - generated by a power failure, or memory parity error.

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**Question 2(c)** (4)

Use a table to make a comparison between at least four characteristics of a Large-Register-File (such as those used in a RISC-type architecture) and those of a typical Cache Organization.

| Large Register File | Cache |
|---|---|
| All local scalars | Recently-used local scalars |
| Individual variables | Blocks of memory |
| Compiler-assigned global variables | Recently-used global variables |
| Save / Restore based on procedure nesting depth | Save / Restore based on cache replacement algorithm |
| Register adressing | Memory addressing |

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**Question 2(d)** (6)

Briefly describe the cache organization of the Pentium 4.

There are 3 caches, 2 of which are on-chip -

- L1 instruction cache (on-chip). 12Kb in size and holds micro operations. Between the instructon decode logic and execution core.
- L1 data cache (on-chip). 8Kb, 4-way set associative organization. Uses a write-block policy.
- L2 cache of 256Kb. Feeds both L1 data and instruction caches. The organization of L2 is 8-way set-associative.

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## May / June 2012

**Question 2(a)** (6)

One of the distinctions among memory types is the *method of accessing* of the data. Briefly discuss three different methods of accessing data.

- **Sequential access** - Access must be made in a specific linear sequence. Time to access an arbitrary record is highly variable. Eg: Tape units.

- **Direct access** - Individual blocks or records have a unique address based on location. Access is accomplished by direct access to reach a general vicinity plus sequential searching, counting, or waiting to reach the final location. Access time is variable. Eg: Disk units.

- **Random access** - Each addressable location in memory has a unique, physically wired-in addressing mechanism. The time to access a given location is constant. Any location can be selected at random, and directly addressed and accessed. Eg: Main memory and some cache systems.

- **Associative** - A random access type of memory that enables one to make a comparison of desired bit locations within a word for a specified match, and do this for all words simultaneously. A word is retrieved based on a portion of its contents rather than its address. Retrieval time is constant. Eg: Cache memories may use associative access.

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**Question 2(b)** (5)

Discuss the advantages and disadvantages of using DMA over programmed and interrupt-driven I/O.

Advantages -
- More efficient when large volumes of data have to be moved.
- Does not cause the processor to wait for long periods of time.
- Does not use processor time to transfer data.

Disadvantages -
- Cycle stealing - DMA forces the processor to suspend operation while it uses the bus.

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**Question 2(d)** (5)

Briefly describe flash memory with special reference to the
(i) density compared to EPROM, and
(II) erasing technology.

(i) Similar density to EPROM - one transistor per bit. (Higher density than EEPROM).

(ii) Electrical erasing technology;
An entire flash memory can be erased in one, or a few, seconds (in a flash).
It is possible to erase blocks of memory, but byte level erasure is not provided for.

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## October / November 2011

**Question 2(a)** (5)

List five of the key elements shared by most designs of RISC architectures.

- One instruction per cycle;
- Register-to-register operations;
- Simple addressing modes;
- Simple instruction formats;
- A single instruction size.

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**Question 2(c)** (5)

There are several steps involved in the execution of an instruction. List at least five of the steps of the general instruction cycle.

- Fetch instruction
- Decode instruction
- Calculate operands
- Fetch operands
- Execute instruction
- Write operands

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**Question 2(d)** (5)

What is meant by the term *programmed I/O*. What is the main disadvantage of using this technique ?

**Programmed I/O** - data are exchanged between the processor and the I/O module. The processor executes a program that gives it direct control of the I/O operation, including sensing device status, sending a read or write command, and transferring the data. When the processor issues a command to the I/O module, it must wait until the I/O operation is complete. If the processor is faster than the I/O module, this is wasteful of processor time.

Disadvantage - The processor has to wait a long time for the I/O module to be ready for either reception or transmission of data. Processor has to repeatedly check the status of the I/O module. This degrades the performance of the entire system.

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**Question 2(c)** (4)

What are the primary differences between SRAM and DRAM ?

SRAM is used for cache memory, DRAM is used for main memory;
SRAM is more expensive and larger than DRAM;
SRAM has faster access times than DRAM;
SRAM is a digital device, DRAM is an analogue device.

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**Question 2(d)** (6)

Explain the difference between a compiler, a translator, and an assembler.

**Compiler** - A program that converts another program from some source language (or programming language) to machine language (object code).

**Translator** - Converts assembly language instruction into binary machine code.

**Assembler** - A program that translates assembly language into machine code.

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